NTMFS5834NL

Power MOSFET

40 V, 74 A, 9.3 mΩ

Features

- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	13	A
		T_A = 100°C		11	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	3.0	W
		T_A = 100°C		1.9	
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	74	A
		T_C = 100°C		59	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	89	W
		T_C = 100°C		57	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	276	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	74	A
Single Pulse Drain−to−Source Avalanche Energy (L = 0.1 mH)			EAS	48	mJ
			IAS	31	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Bottom) (Note 1)	$R_{\theta JC}$	1.4	°C/W
Junction−to−Case (Top) (Note 1)	$R_{\theta JC}$	4.5	
Junction−to−Ambient Steady State (Note 1)	$R_{\theta JA}$	41	
Junction−to−Ambient Steady State (Note 2)	$R_{\theta JA}$	75	

1. Surface−mounted on FR4 board using 1 sq−in pad (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface−mounted on FR4 board using 0.155 in sq (100mm^2) pad size.

ON Semiconductor®

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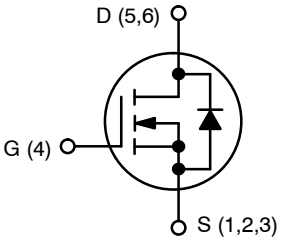
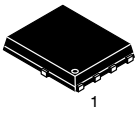
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	9.3 mΩ @ 10 V	74 A
	13.6 mΩ @ 4.5 V	

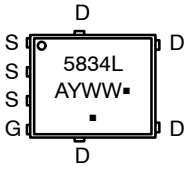


N−CHANNEL MOSFET



DFN5
(SO−8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS5834NLT1G	DFN5 (Pb−Free)	1500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				34.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A		7.1	9.3	mΩ
		V_{GS} = 4.5 V	I_D = 20 A		11.3	13.6	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 20 A			29		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V			1231		pF
Output Capacitance	C_{OSS}				198		
Reverse Transfer Capacitance	C_{RSS}				141		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 20 A			24		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 20 A			12		
Threshold Gate Charge	$Q_{G(TH)}$				1.0		
Gate−to−Source Charge	Q_{GS}				4.2		
Gate−to−Drain Charge	Q_{GD}				6.3		
Plateau Voltage	V_{GP}				3.4		V
Gate Resistance	R_G				0.7		Ω
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 20 A, R_G = 2.5 Ω			10		ns
Rise Time	t_r				56.4		
Turn−Off Delay Time	$t_{d(OFF)}$				17.4		
Fall Time	t_f				6.6		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.84	1.2	V
			T_J = 125°C		0.72		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 20 A			18		ns
Charge Time	t_a				10		
Discharge Time	t_b				8.0		
Reverse Recovery Charge	Q_{RR}				108		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

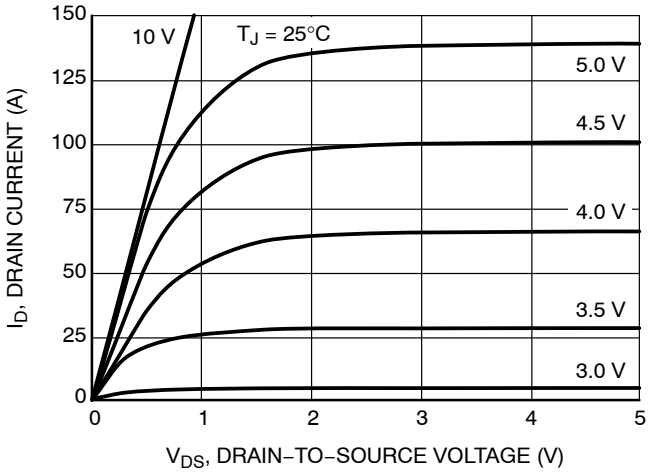


Figure 1. On−Region Characteristics

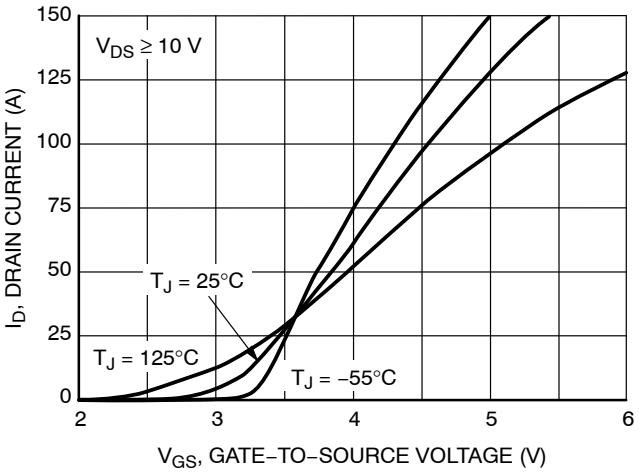


Figure 2. Transfer Characteristics

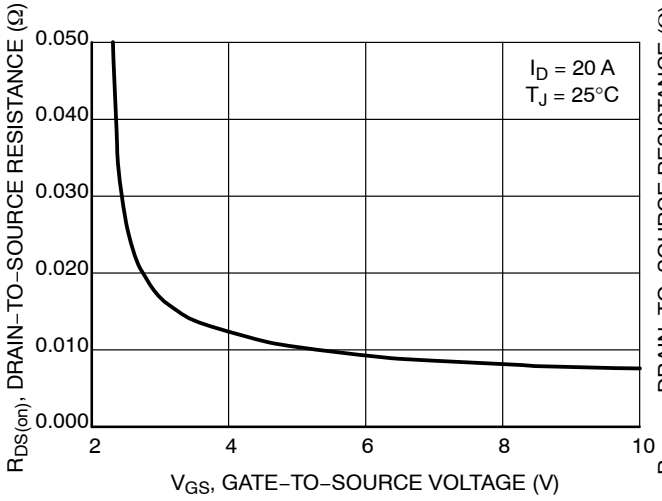


Figure 3. On−Resistance vs. Gate−to−Source Voltage

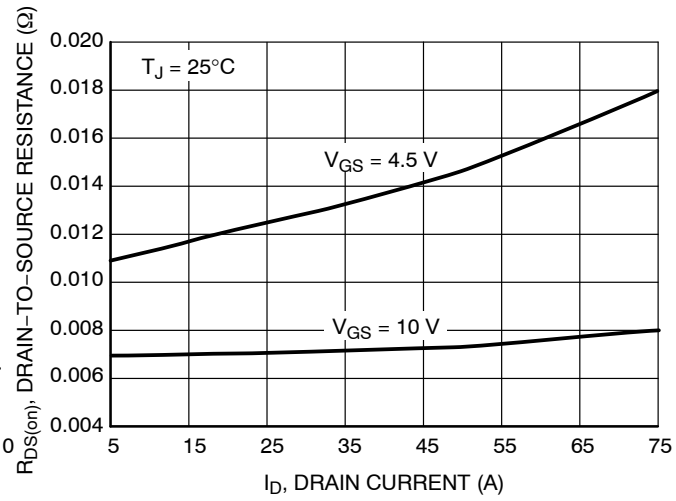


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

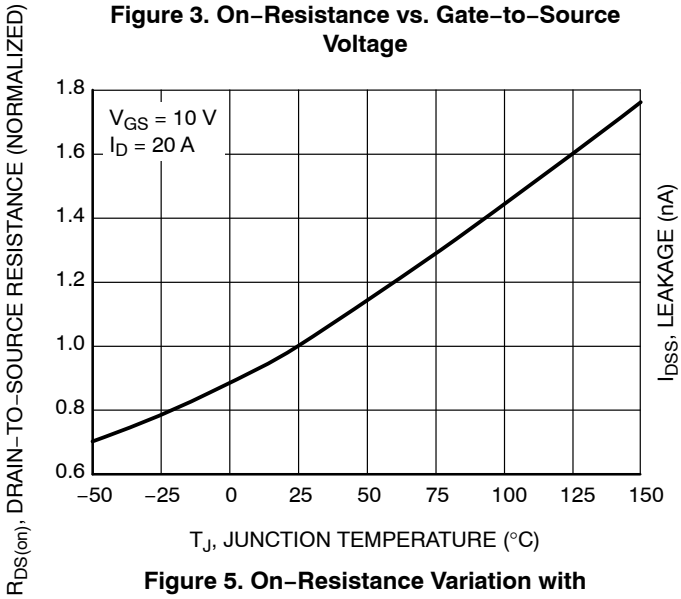


Figure 5. On−Resistance Variation with Temperature

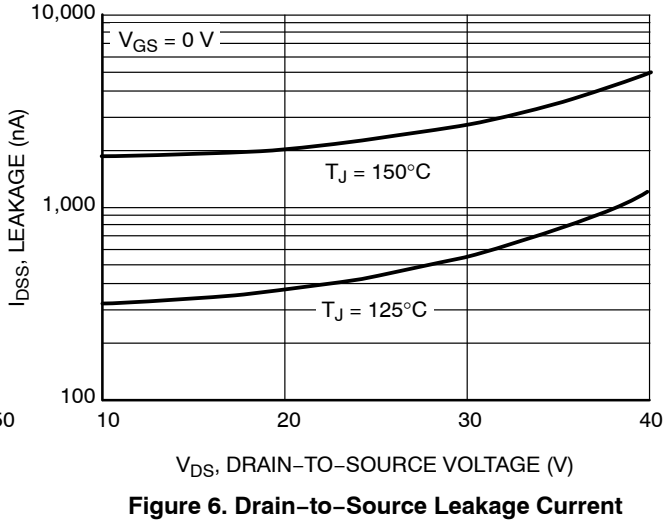


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

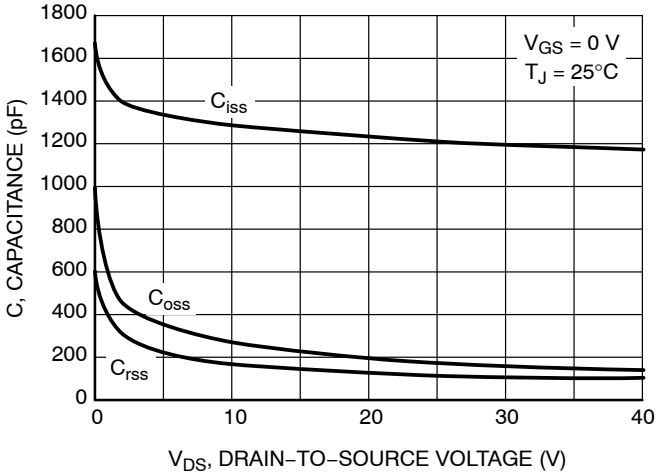


Figure 7. Capacitance Variation

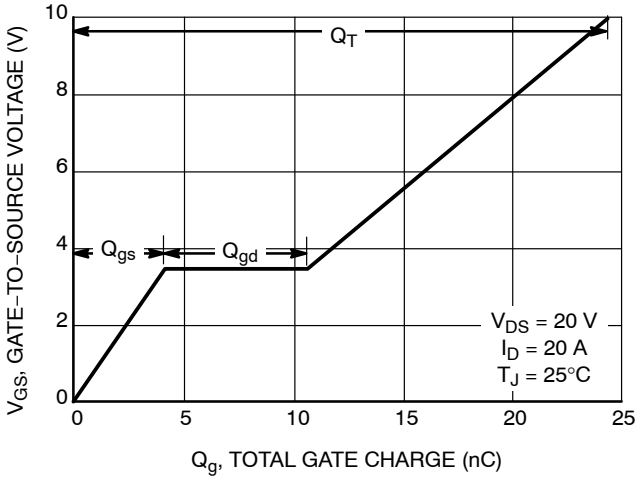


Figure 8. Gate−to−Source Voltage vs. Total Charge

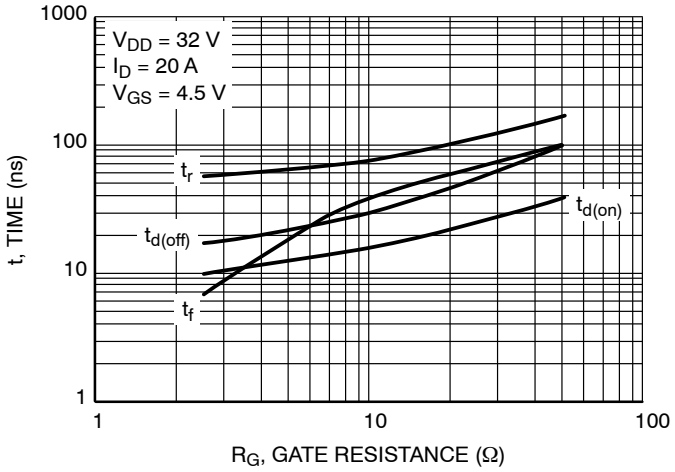


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

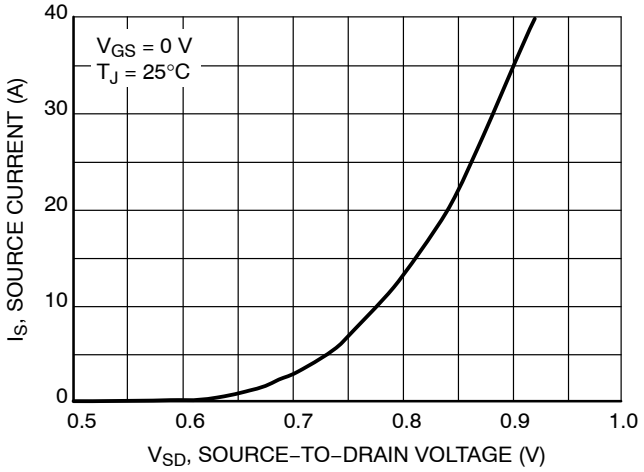


Figure 10. Diode Forward Voltage vs. Current

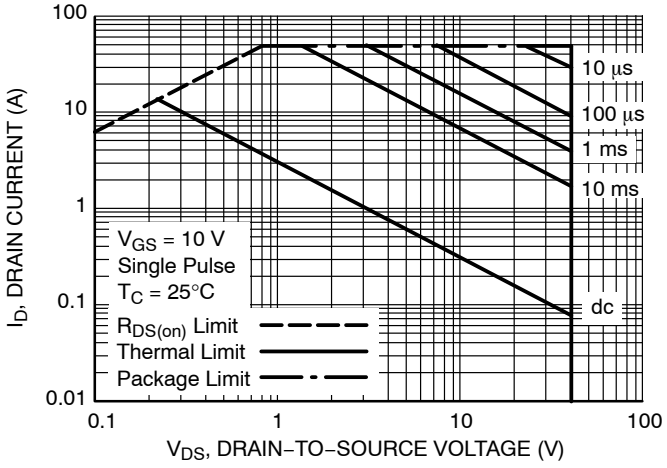


Figure 11. Maximum Rated Forward Biased Safe Operating Area

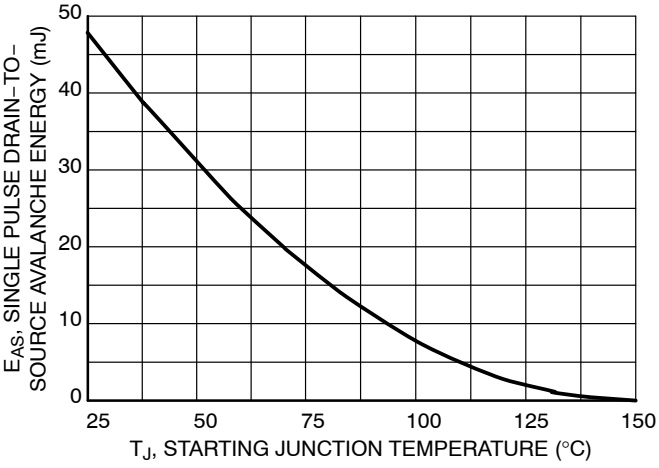


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

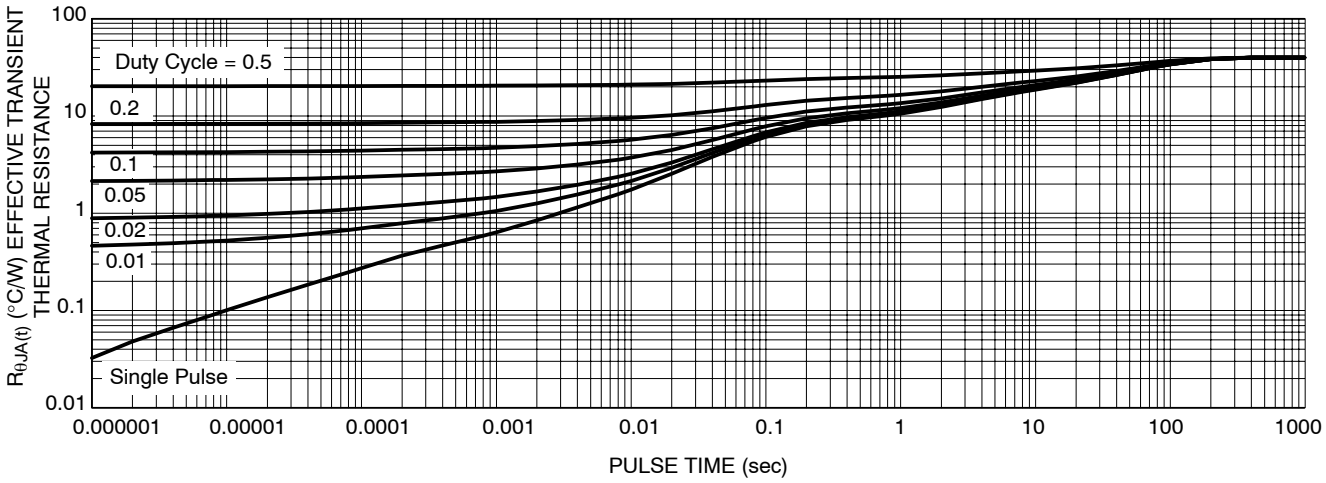
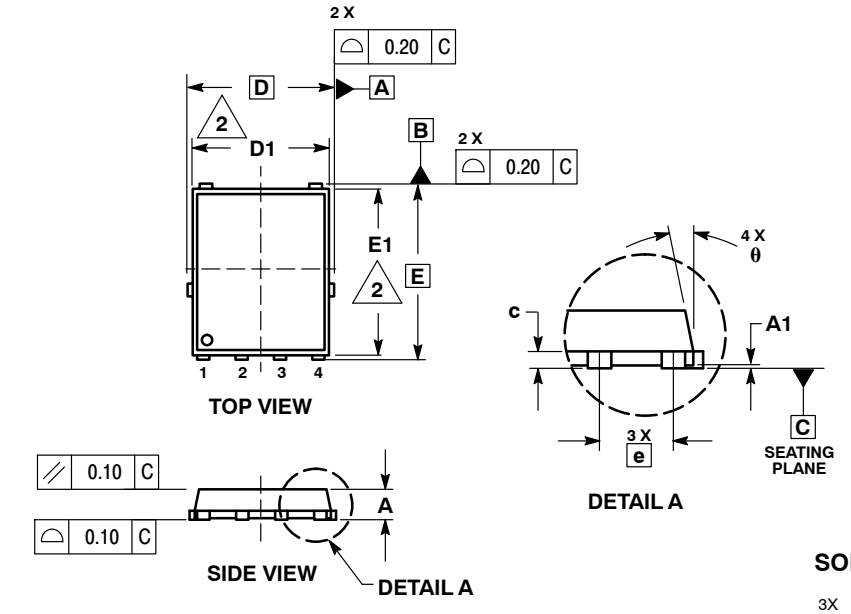
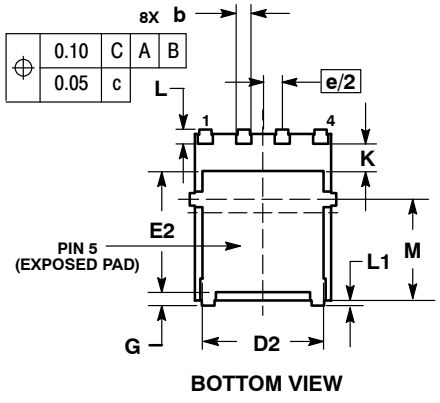


Figure 13. Thermal Response

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA−01
ISSUE D



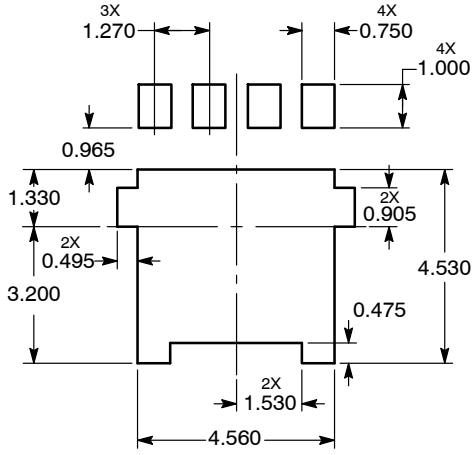


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.50	4.90	5.10
D2	3.50	−−−	4.22
E		6.15 BSC	
E1	5.50	5.80	6.10
E2	3.45	−−−	4.30
e		1.27 BSC	
G	0.51	0.61	0.71
K	0.51	−−−	−−−
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	−−−	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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